FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11220-1E

MEMORY

CMOS 2M × 64
FAST PAGE MODE DRAM MODULE

MB8502D064AA-60/-70

CMOS 2M × 64 Bit Fast Page Mode DRAM Module

■ DESCRIPTION

The Fujitsu MB8502D064AA is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117800A devices. The MB8502D064AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8502D064AA are the same as the MB8117800A which features fast page mode operation. For ease of memory expansion, the MB8502D064AA is offered in an 168-pad Dual In-line Memory Module package (DIMM).

■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	10	W
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Parameter		MB8502D064AA-60	MB8502D064AA-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		110 ns max.	130 ns max.
Address Access Time		35 ns max.	40 ns max.
$\overline{CAS}$ Access Time		20 ns min.	22 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Power Dissipation	Operating Mode	6600 mW max.	6105 mW max.
	Standby Mode	440 mW max.	440 mW max.

- Conformed to 8-Byte DIMM JEDEC standard
- Organization : 2,097,152 words × 64 bits
- Module Size : 1.00” (height) × 5.25” (length) × 0.350” (thick)
- Memory : MB8117800A (2M × 8, 2K ref.), 8 pcs
- TI’s Input Buffers, 2 pcs
- TI’s Input Driver for Buffered PD, 1pc
- Decoupling Capacitors, 10 pcs
- 5.0 V ± 10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Fast Page operation
- $\overline{RAS}$ Only Refresh / $\overline{CAS}$-before-$\overline{RAS}$ Refresh
- Package and Ordering Information:
  168-pad DIMM, order as
  MB8502D064AA-xxDG (DG = Gold Pad)

■ PACKAGE

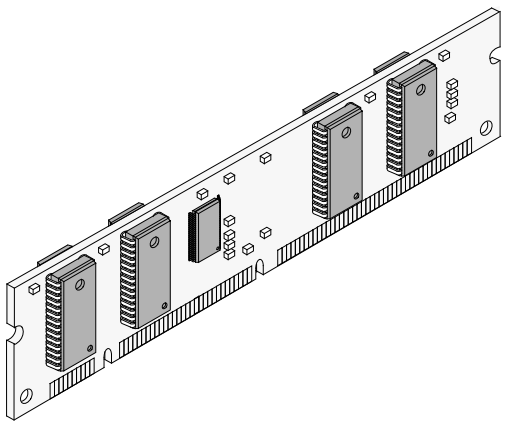

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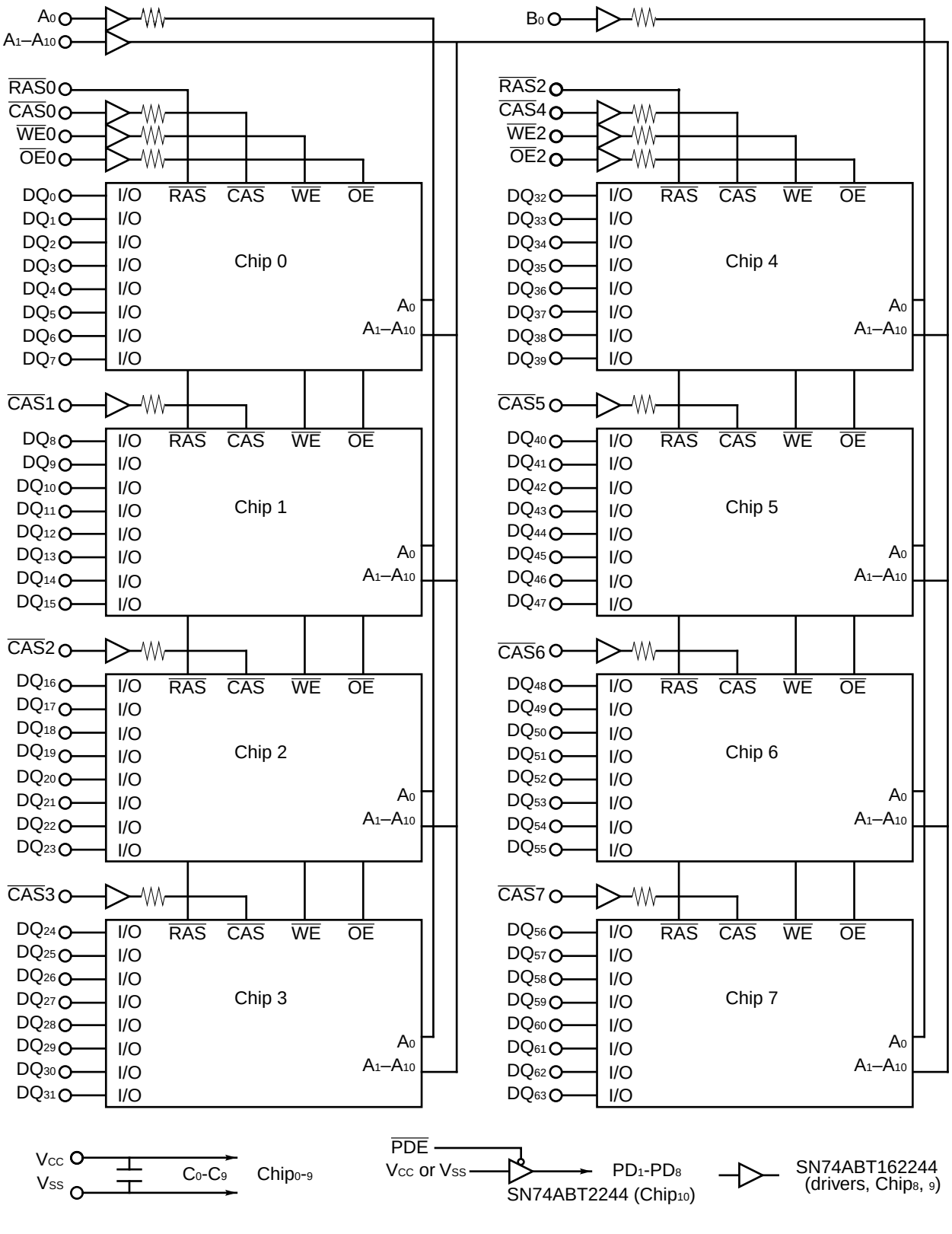
Fig. 1 – BLOCK DIAGRAM



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■ PIN ASSIGNMENTS

Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA
1	V_{SS}	36	A_6	71	DQ_{27}	106	NC
2	DQ_0	37	A_8	72	DQ_{28}	107	V_{SS}
3	DQ_1	38	A_{10}	73	V_{CC}	108	NC
4	DQ_2	39	NC	74	DQ_{29}	109	NC
5	DQ_3	40	V_{CC}	75	DQ_{30}	110	V_{CC}
6	V_{CC}	41	NC	76	DQ_{31}	111	NC
7	DQ_4	42	NC	77	NC	112	$\overline{CAS}1$
8	DQ_5	43	V_{SS}	78	V_{SS}	113	$\overline{CAS}3$
9	DQ_6	44	$\overline{OE}2$	79	PD_1	114	NC
10	DQ_7	45	$\overline{RAS}2$	80	PD_3	115	NC
11	NC	46	$\overline{CAS}4$	81	PD_5	116	V_{SS}
12	V_{SS}	47	$\overline{CAS}6$	82	PD_7	117	A_1
13	DQ_8	48	$\overline{WE}2$	83	ID_0	118	A_3
14	DQ_9	49	V_{CC}	84	V_{CC}	119	A_5
15	DQ_{10}	50	NC	85	V_{SS}	120	A_7
16	DQ_{11}	51	NC	86	DQ_{32}	121	A_9
17	DQ_{12}	52	DQ_{16}	87	DQ_{33}	122	NC
18	V_{CC}	53	DQ_{17}	88	DQ_{34}	123	NC
19	DQ_{13}	54	V_{SS}	89	DQ_{35}	124	V_{CC}
20	DQ_{14}	55	DQ_{18}	90	V_{CC}	125	NC
21	DQ_{15}	56	DQ_{19}	91	DQ_{36}	126	B_0
22	NC	57	DQ_{20}	92	DQ_{37}	127	V_{SS}
23	V_{SS}	58	DQ_{21}	93	DQ_{38}	128	NC
24	NC	59	V_{CC}	94	DQ_{39}	129	NC
25	NC	60	DQ_{22}	95	NC	130	$\overline{CAS}5$
26	V_{CC}	61	NC	96	V_{SS}	131	$\overline{CAS}7$
27	$\overline{WE}0$	62	NC	97	DQ_{40}	132	$\overline{PDE}$
28	$\overline{CAS}0$	63	NC	98	DQ_{41}	133	V_{CC}
29	$\overline{CAS}2$	64	NC	99	DQ_{42}	134	NC
30	$\overline{RAS}0$	65	DQ_{23}	100	DQ_{43}	135	NC
31	$\overline{OE}0$	66	NC	101	DQ_{44}	136	DQ_{48}
32	V_{SS}	67	DQ_{24}	102	V_{CC}	137	DQ_{49}
33	A_0	68	V_{SS}	103	DQ_{45}	138	V_{SS}
34	A_2	69	DQ_{25}	104	DQ_{46}	139	DQ_{50}
35	A_4	70	DQ_{26}	105	DQ_{47}	140	DQ_{51}

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(Continued)

Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA	Pin No.	MB8502D064AA
141	DQ_{52}	148	NC	155	DQ_{59}	162	V_{SS}
142	DQ_{53}	149	DQ_{55}	156	DQ_{60}	163	PD_2
143	V_{CC}	150	NC	157	V_{CC}	164	PD_4
144	DQ_{54}	151	DQ_{56}	158	DQ_{61}	165	PD_6
145	NC	152	V_{SS}	159	DQ_{62}	166	PD_8
146	NC	153	DQ_{57}	160	DQ_{63}	167	ID_1
147	NC	154	DQ_{58}	161	NC	168	V_{CC}

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■ PIN DESCRIPTIONS

Symbol	Function	Input/Output	Pin Count
A_0 to A_{10}, B_0	Address Input	Input	12
$\overline{RAS}0$ and $\overline{RAS}2$	Row Address Strobe	Input	2
$\overline{CAS}0$ to $\overline{CAS}7$	Column Address Strobe	Input	8
$\overline{WE}0$ and $\overline{WE}2$	Write Enable	Input	2
$\overline{OE}0$ and $\overline{OE}2$	Output Enable	Input	2
DQ_0 to DQ_{63}	Data-input/Data-output	Input/Output	64
PD_1 to PD_8	Presence Detect	Output	8
ID_0 and ID_1	ID bit	Output	2
$\overline{PDE}$	Presence Detect Enable	Input	1
V_{CC}	Power Supply	—	16
V_{SS}	Ground	—	16
NC	No Connection	—	35

■ PRESENCE DETECT (PD)/ID DEFINITION

Symbol	MB8502D064AA-60	MB8502D064AA-70	Description of PD/ID
PD_1	H	H	MODULE DENSITY, DRAM ORGANIZATION AND ADDRESSING; Module Density: 16MB, Number of Bank: 1 Bank Module Configuration: 2M × 64 Mounted DRAM Configuration: 2M × 8 DRAM Address (Row/Column): 11/10
PD_2	L	L	
PD_3	L	L	
PD_4	H	H	
PD_5	L	L	EDO DETECTION; Fast Page Mode : PD_5 = L
PD_6	H	L	MODULE SPEED; 60 ns : PD_6 = H, PD_7 = H 70 ns : PD_6 = L, PD_7 = H
PD_7	H	H	
PD_8	H	H	ECC / PARITY DETECTION; (parity) : PD_8 = H
ID_0	L	L	MODULE TYPE; ×64 (parity) : ID_0 = L
ID_1	H	H	REFRESH MODE; Self Refresh : ID_1 = L

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = +5.0 V)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance, (Address)	C_{IN1}	—	20	pF
Input Capacitance ($\overline{RAS}$)	C_{IN2}	—	50	pF
Input Capacitance, ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN3}	—	20	pF
I/O Capacitance, (DQ)	C_{DQ}	—	20	pF

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.0	V
Input Low Voltage, all inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

Note: *Undershoots of up to –1.5 volts with a pulse width not exceeding 10 ns are acceptable.

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Test Condition	Symbol	Min.	Max.	Unit
Output High Voltage*1		I_{OH} = –5 mA	V_{OH}	2.4	—	V
Output Low Voltage*1		I_{OL} = 4.2 mA	V_{OL}	—	0.4	V
Input Leakage Current	$\overline{RAS}$	0 V ≤ V_{IN} ≤ 5.5 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, V_{SS} = 0 V, all other pins not under test = 0 V	$I_{I(L)}$	–30	30	µA
	Others			–10	10	
Output Leakage Current		0 V ≤ V_{OUT} ≤ 5.5 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, Data out disabled	$I_{O(L)}$	–10	10	µA
Operating Current*2 (Average Power Supply Current)	MB8502D064AA-60	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min.	I_{CC1}	—	1200	mA
	MB8502D064AA-70			—	1110	
Standby Current*2 (Power Supply Current)	TTL Level	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{PDE}$=V_{IH}	I_{CC2}	—	80	mA
	CMOS Level	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{PDE}$ ≥V_{CC}–0.2 V		—	69	
Refresh Current #1*2 (Average Power Supply Current)	MB8502D064AA-60	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min.	I_{CC3}	—	1200	mA
	MB8502D064AA-70			—	1110	
Fast Page Mode Current*2	MB8502D064AA-60	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{RC} = min.	I_{CC4}	—	1147	mA
	MB8502D064AA-70			—	1056	
Refresh Current #2*2 (Average Power Supply Current)	MB8502D064AA-60	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.	I_{CC5}	—	1120	mA
	MB8502D064AA-70			—	1030	
Refresh Current #3 (Average Power Supply Current)		Self-Refresh; A_0-A_{10}, B_0, $\overline{WE}$, $\overline{OE}$, $\overline{PDE}$ ≥ V_{CC}–2.1 V	I_{CC9}	—	30	mA

Notes: *1: Referenced to V_{SS}.

*2: I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3 V.

I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

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■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB8502D064AA-60		MB8502D064AA-70		Unit	Notes
			Min.	Max.	Min.	Max.		
1	Time Between Refresh	t_{REF}	—	32.8	—	32.8	ms	
2	Random Read/Write Cycle Time	t_{RC}	110	—	130	—	ns	
3	Read-Modify-Write Cycle Time	t_{RWC}	150	—	174	—	ns	
4	Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	4, 7
5	Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	22	ns	5, 7
6	Column Address Access Time	t_{AA}	—	35	—	40	ns	6, 7
7	Output Hold Time	t_{OH}	5	—	5	—	ns	
8	Output Buffer Turn On Delay Time	t_{ON}	2	—	2	—	ns	
9	Output Buffer Turn Off Delay Time	t_{OFF}	—	20	—	22	ns	8
10	Transition Time	t_T	2	16	2	16	ns	
11	$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
12	$\overline{RAS}$ Pulse Width	t_{RAS}	60	100000	70	100000	ns	
13	$\overline{RAS}$ Hold Time	t_{RSH}	20	—	22	—	ns	
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	ns	
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	18	40	18	48	ns	9, 10
16	$\overline{CAS}$ Pulse Width	t_{CAS}	15	—	17	—	ns	
17	$\overline{CAS}$ Hold Time	t_{CSH}	58	—	68	—	ns	
18	$\overline{CAS}$ Precharge Time (C-B-R Refresh)	t_{CPN}	10	—	10	—	ns	17
19	Row Address Setup Time	t_{ASR}	5	—	5	—	ns	
20	Row Address Hold Time	t_{RAH}	8	—	8	—	ns	
21	Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
22	Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
23	Column Address Hold Time from $\overline{RAS}$	t_{AR}	33	—	33	—	ns	
24	$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	13	25	13	30	ns	11
25	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	ns	
26	Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	ns	
27	Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
28	Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	–2	—	–2	—	ns	12
29	Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
30	Write Command Setup Time	t_{WCS}	0	—	0	—	ns	13, 18
31	Write Command Hold Time	t_{WCH}	15	—	15	—	ns	
32	Write Command Hold Timefrom $\overline{RAS}$	t_{WCR}	33	—	33	—	ns	

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(Continued)

No.	Parameter	Symbol	MB8502D064AA-60		MB8502D064AA-70		Unit	Notes
			Min.	Max.	Min.	Max.		
33	$\overline{WE}$ Pulse Width	t_{WP}	15	—	15	—	ns	
34	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	22	—	ns	
35	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	17	—	ns	
36	D_{IN} Setup Time	t_{DS}	–2	—	–2	—	ns	
37	D_{IN} Hold Time	t_{DH}	20	—	20	—	ns	
38	Data Hold Time from $\overline{RAS}$	t_{DHR}	35	—	35	—	ns	
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	78	—	90	—	ns	18
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	39	—	ns	18
41	Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	57	—	ns	18
42	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	3	—	3	—	ns	
43	$\overline{CAS}$ Setup Time (C-B-R Refresh)	t_{CSR}	5	—	5	—	ns	
44	$\overline{CAS}$ Hold Time (C-B-R Refresh)	t_{CHR}	8	—	10	—	ns	
45	Access Time from $\overline{OE}$	t_{OEA}	—	20	—	22	ns	7
46	Output Buffer Turn Off Delay from $\overline{OE}$	t_{OEZ}	—	20	—	22	ns	8
47	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	t_{OEL}	15	—	15	—	ns	
48	$\overline{OE}$ Hold Time Referencedto $\overline{WE}$	t_{OEH}	5	—	5	—	ns	14
49	$\overline{OE}$ to Data in Delay Time	t_{OED}	20	—	22	—	ns	
50	$\overline{CAS}$ to Data in Delay Time	t_{CDD}	20	—	22	—	ns	
51	DIN to $\overline{CAS}$ Delay Time	t_{DZC}	–2	—	–2	—	ns	15
52	DIN to $\overline{OE}$ Delay Time	t_{DZO}	–2	—	–2	—	ns	15
53	Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	ns	
54	Fast Page Mode Read/Write Cycle Time	t_{PC}	40	—	45	—	ns	
55	Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	80	—	89	—	ns	
56	Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	40	—	45	ns	7, 16
57	Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
58	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	ns	
59	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	55	—	62	—	ns	18
60	$\overline{RAS}$ Pulse Width (Self Refresh)	t_{RASS}	100	—	100	—	µs	19
61	$\overline{RAS}$ Precharge Time (Self Refresh)	t_{RPS}	110	—	125	—	ns	19
62	$\overline{CAS}$ Hold Time (Self Refresh)	t_{CHS}	–52	—	–52	—	ns	19

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Notes:
1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max.) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min.) = t_{RAH} (min.)+ 2 t_T + t_{ASC} (min.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min.) the data output pin will remain High-Z state through entire cycle.
14. Assumes that $t_{WCS} < t_{WCS}$ (min.).
15. Either t_{DZC} or t_{DZO} must be satisfied.
16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max.).
17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
18. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.), $t_{RWD} \geq t_{RWD}$(min.), $t_{AWD} \geq t_{AWD}$ (min.), and $t_{CPWD} \geq t_{CPWD}$ (min.), the cycle is a read- modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} specifications.
19. Assumes that self refresh.

*Source: See MB8117800A Data Sheet for details on the electricals.

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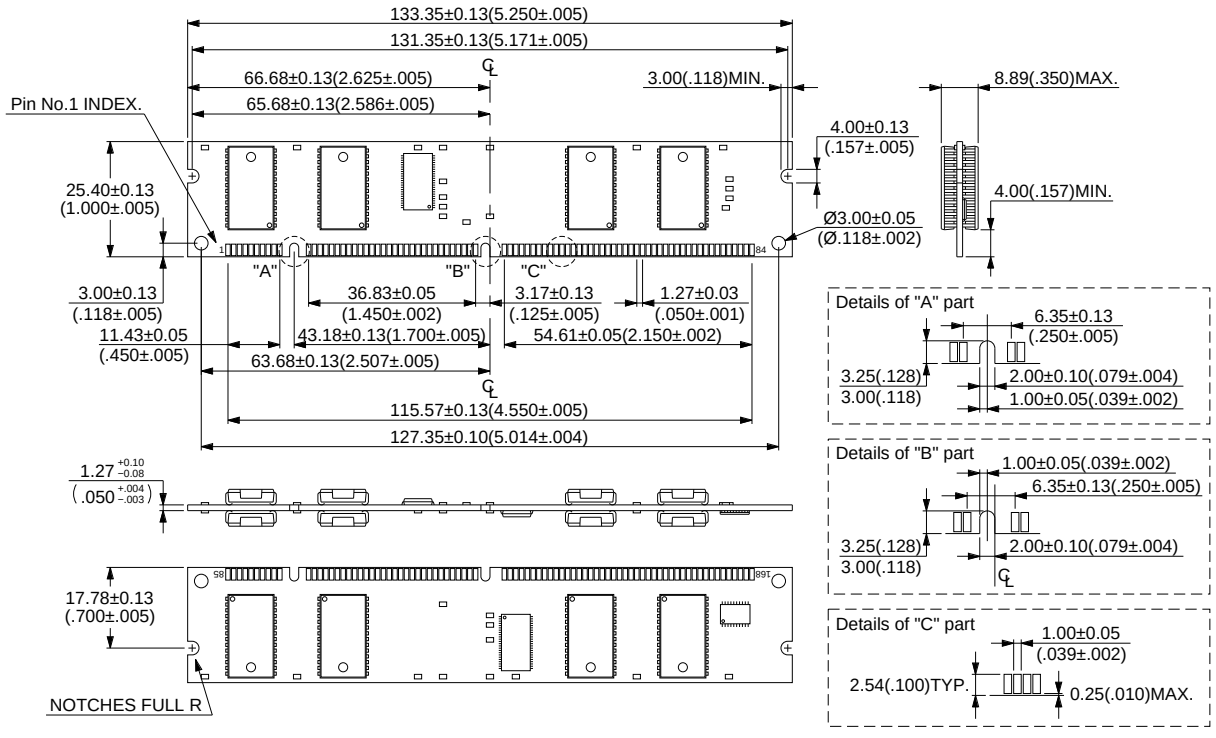
■ PACKAGE DIMENSIONS

(Suffix: DG)

168 pin, Plastic DIMM
(MDS-168P-P06)



Dimensions in mm(inches).

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Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.